3GHz to 8GHz High Linearity Active Upconverting Mixer

FEATURES

- **25dBm OIP3**
- **–0.6dB Conversion Gain**
- **14.1dB Noise Figure at 5.8GHz**
- **–154dBm/Hz Output Noise Floor**
- **Low LO-RF Leakage**
- **0dBm LO Drive**
- **Broadband 50Ω Matched Input**
- **High Input P1dB: 10dBm at 5V**
- **5V or 3.3V Supply at 99mA**
- **Single-Ended Output and LO Input**
- Enable Pin
- –40°C to 105°C Operation (T_C)
- 16-Lead (4mm × 4mm) QFN Package

APPLICATIONS

- Wideband Transmitters
- 4G and 5G Wireless Infrastructure
- Fixed Wireless Access Equipment
- Wireless Repeaters

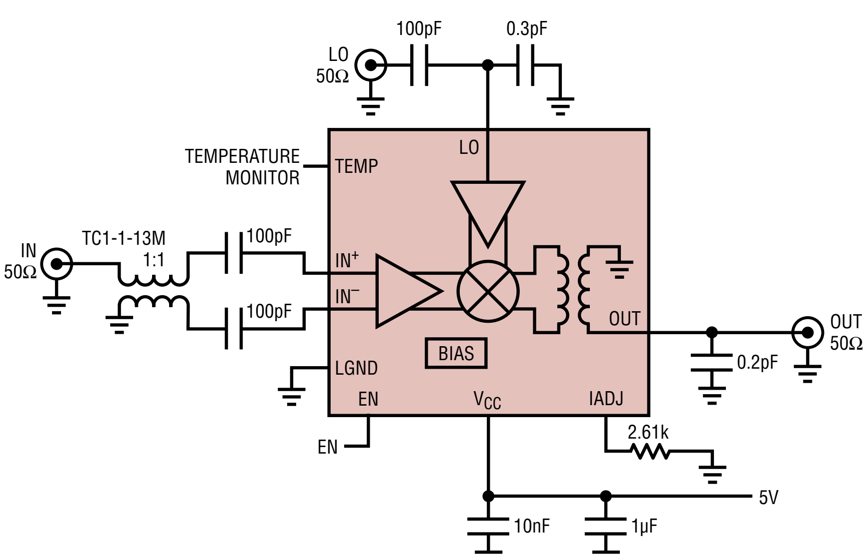
DESCRIPTION

The LTC®5576 is a high linearity active mixer optimized for upconverting applications requiring wide input bandwidth, low distortion and low LO leakage. The integrated output transformer is optimized for 4GHz to 6GHz applications, but is easily retuned for output frequencies as low as 3GHz, or as high as 8GHz, with minor performance degradation. The input is optimized for use with 1:1 transmission-line baluns, allowing very wideband impedance matching.

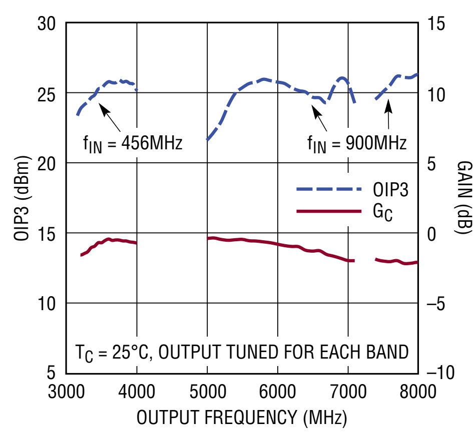
The LO input port is single-ended and requires only 0dBm of LO power to achieve excellent distortion and noise performance while also reducing circuit requirements. The LTC5576 offers low LO leakage, reducing the demands of output filtering to meet LO suppression requirements.

The LTC5576 is optimized for 5V but can also be used with a 3.3V supply with slightly reduced performance. The enable function allows the part to be easily shut down for further power savings.

TYPICAL APPLICATION



OIP3 and Conversion Gain vs Output Frequency (LSLO)

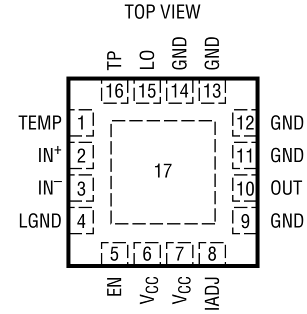


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
Enable Voltage ....–0.3V to V_{CC} + 0.3V
IADJ Pin Voltage ....–0.3 to 2.7V
LO Input Power (1GHz to 8GHz)......................... +10dBm
IN^+, IN^- Input Power (30MHz to 6GHz).............. +15dBm
TEMP Input Current 10mA
Operating Temperature Range (T_C)........ –40°C to 105°C
Junction Temperature (T_J) .... 150°C
Storage Temperature Range .... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 6°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5576IUF#PBF	LTC5576IUF#TRPBF	5576	16-Lead (4mm × 4mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C, V_{CC} = 5V. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})	5V Supply 3.3V Supply	● ●	4.5 3.1	5 3.3	5.3 3.5	V V
Supply Current	5V, R1 = 2.61kΩ 3.3V, R1 = 649Ω Shutdown (EN = Low)			99 85 1.3	112	mA mA mA
Enable Logic Input (EN)						
EN Input High Voltage (On)			1.8			V
EN Input Low Voltage (Off)					0.5	V
EN Input Current	–0.3V to V_{CC} + 0.3V		–20		200	µA
Turn-On Time				0.6		µs
Turn-Off Time				0.6		µs
Current Adjust Pin (IADJ)						
Open Circuit DC Voltage				1.8		V
Short Circuit DC Current				1.9		mA
Temperature Sensing Diode (TEMP)						
DC Voltage at T_J = 25°C	I_{IN} = 10µA I_{IN} = 80µA			697 755		mV mV
Voltage Temperature Coefficient	I_{IN} = 10µA I_{IN} = 80µA			–1.80 –1.61		mV/°C mV/°C

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 5V, EN = High, P_{LO} = 0dBm. Test circuit shown in Figure 1. (Notes 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LO Input Frequency Range	External Matching Required	●		1 to 8		GHz
Input (IN) Frequency Range	External Matching Required	●		0.03 to 6		GHz
Output (OUT) Frequency Range	External Matching Required	●		3 to 8		GHz
Input Return Loss	Z_0 = 50Ω			>10		dB
LO Input Return Loss	Z_0 = 50Ω			>10		dB
LO Input Power	Single-Ended	●	–6	0	6	dBm
LO to IN Leakage	f_{LO} = 1GHz to 8GHz			≤–30		dBm
IN to LO Isolation	f_{IN} = 0.1GHz to 6GHz			>35		dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 5V, EN = High, P_{IN} = –10dBm (–10dBm/Tone for 2-tone tests, Δf = 2MHz), P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3 and 4)

5V Upmixer Application: Low Side LO, P_{LO}, = 0dBm, P_{IN} = –10dBm

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Gain	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz		 –1.5 	–0.6 –0.6 –2.0	 0.7 	dB dB dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, f_{OUT} = 5.8GHz	●		–0.009		dB/°C
Output 3rd Order Intercept	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			25 25 25		dBm dBm dBm
SSB Noise Figure	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			12.4 14.1 17.5		dB dB dB
SSB Noise Floor at P_{IN} = 5dBm	f_{IN} = 1GHz, f_{OUT} = 5801MHz, f_{LO} = 4899MHz			–154		dBm/Hz
Input 1dB Compression	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			10.8 10.4 10.3		dBm dBm dBm
LO-OUT Leakage	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			–36 –35 –28		dBm dBm dBm
IN to OUT Isolation	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			70 38 35		dB dB dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = High, P_{IN} = –10dBm (–10dBm/Tone for 2-tone tests, Δf = 2MHz), P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3 and 4)

3.3V Upmixer Application: Low Side LO, P_{LO}, = 0dBm, P_{IN} = –10dBm

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Gain	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			–0.6 –0.6 –2.0		dB dB dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, f_{OUT} = 5.8 GHz	●		–0.009		dB/°C
Output 3rd Order Intercept	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			21 23 19		dBm dBm dBm
SSB Noise Figure	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			11.5 12.8 17.8		dB dB dB
SSB Noise Floor at P_{IN} = 5dBm	f_{IN} = 1GHz, f_{OUT} = 5801MHz, f_{LO} = 4899MHz			–154		dBm/Hz
Input 1dB Compression	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} =4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			8.4 8.5 8.1		dBm dBm dBm
LO-OUT Leakage	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			–39 –36 –27		dBm dBm dBm
IN to OUT Isolation	f_{IN} = 456MHz, f_{OUT} = 3.5GHz, f_{LO} = 3.044GHz f_{IN} = 900MHz, f_{OUT} = 5.8GHz, f_{LO} = 4.9GHz f_{IN} = 900MHz, f_{OUT} = 8GHz, f_{LO} = 7.1GHz			70 38 33		dB dB dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

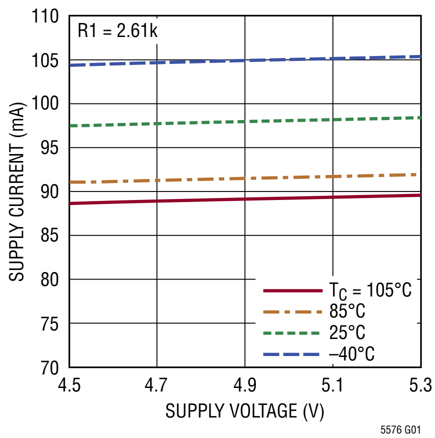
Note 2: The LTC5576 is guaranteed functional over the –40°C to 105°C case temperature range.

Note 3: SSB noise figure measured with a small-signal noise source, bandpass filter and 3dB matching pad on IN port, and bandpass filter on the LO input.

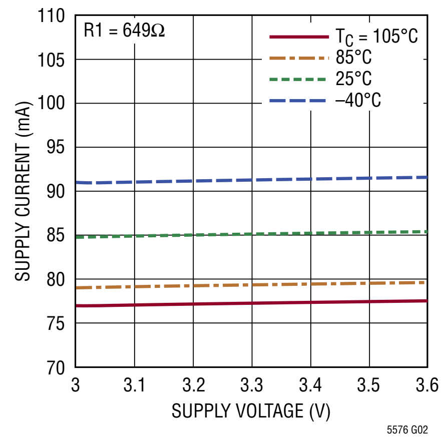
Note 4: Specified performance includes all external component and evaluation PCB losses.

TYPICAL DC PERFORMANCE CHARACTERISTICS (Test Circuit shown in Figure 1)

5V Supply Current vs Supply Voltage



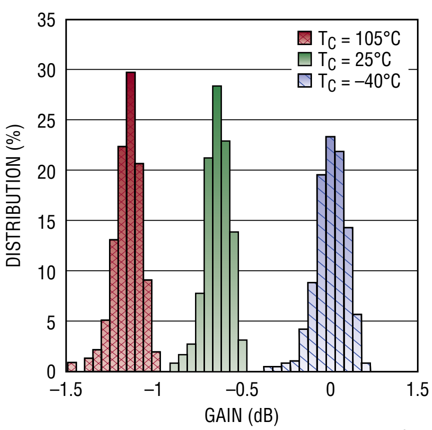
3.3V Supply Current vs Supply Voltage



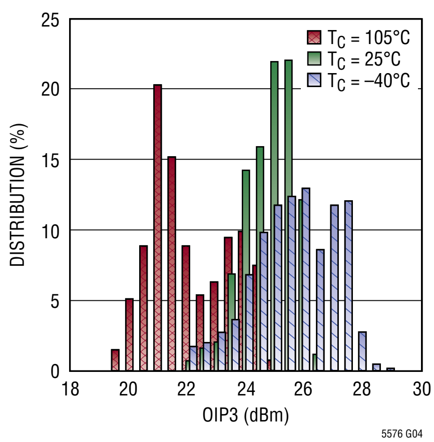
TYPICAL AC PERFORMANCE CHARACTERISTICS 5V, 5800MHz Output Frequency:

T_C = 25°C. V_{CC} = 5V, EN = High, P_{IN} = –10dBm (–10dBm/Tone for 2-tone tests, Δf = 2MHz), P_{LO} = 0dBm, f_{IN} = 900MHz, unless otherwise noted.
Test circuit shown in Figure 1.

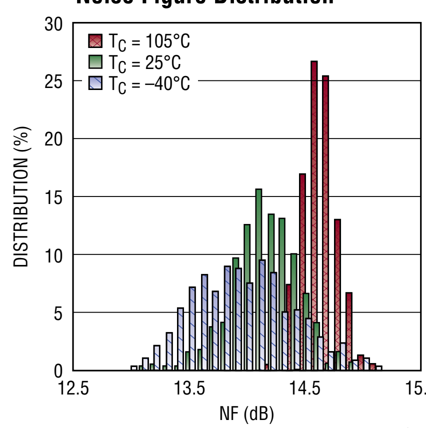
Conversion Gain Distribution



OIP3 Distribution



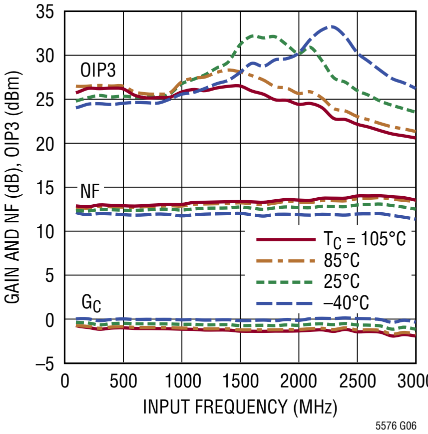
Noise Figure Distribution



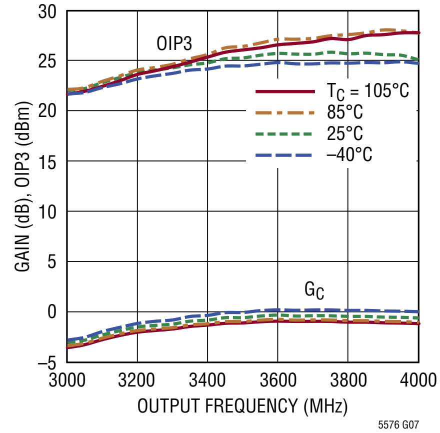
TYPICAL AC PERFORMANCE CHARACTERISTICS

5V, 3500MHz Output Frequency: T_C = 25°C. V_{CC} = 5V, EN = High, P_{IN} = –10dBm (–10dBm/Tone for 2-tone tests, Δf = 2MHz), P_{LO} = 0dBm, f_{IN} = 456MHz, f_{LO} = f_{OUT} – f_{IN}, unless otherwise noted. Test circuit shown in Figure 1.

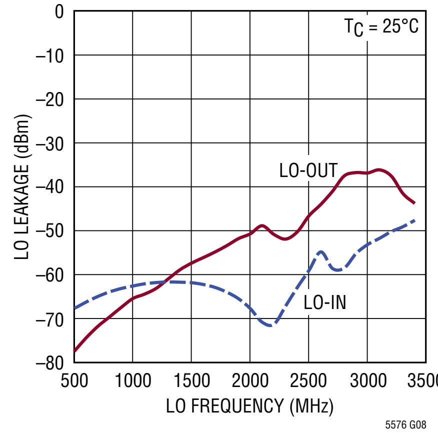
Conversion Gain, OIP3 and NF vs Input Frequency



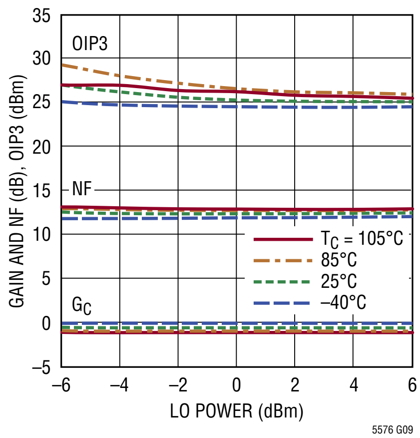
Conversion Gain and OIP3 vs Output Frequency



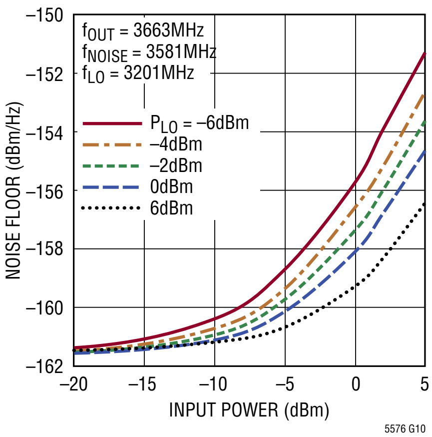
LO Leakage vs LO Frequency



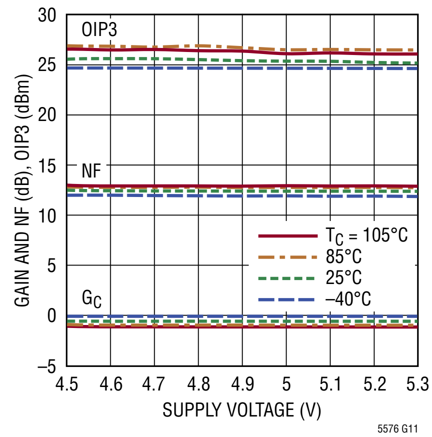
Conversion Gain, OIP3 and NF vs LO Input Power



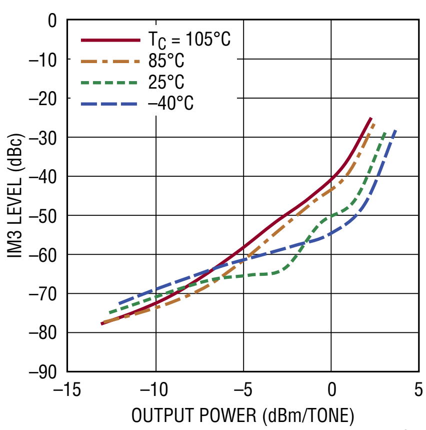
Output Noise Floor vs Input Power



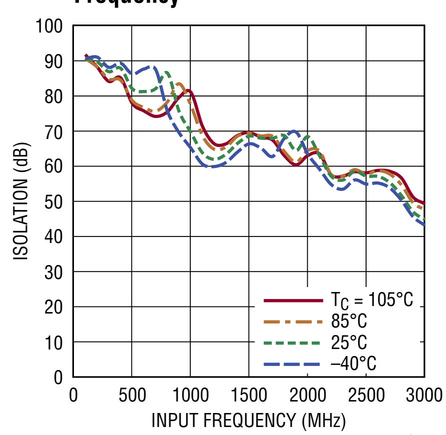
Conversion Gain, OIP3 and NF vs Supply Voltage



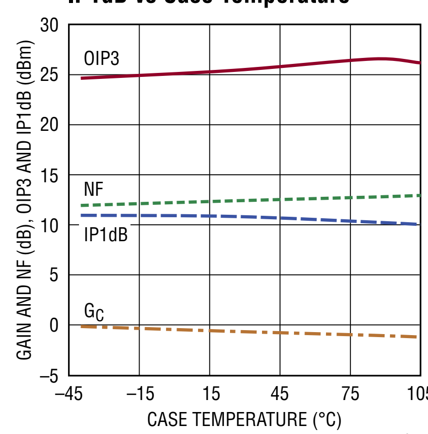
2-Tone IM3 Level vs Output Power Level



IN-OUT Isolation vs Input Frequency



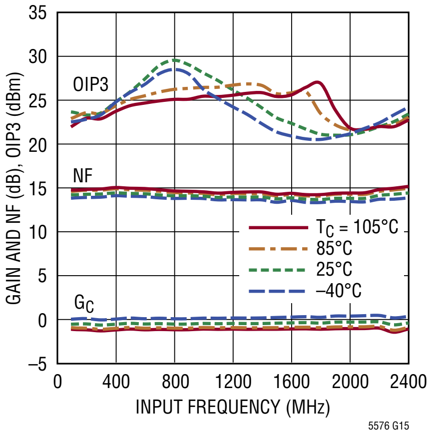
Conversion Gain, OIP3, NF and IP1dB vs Case Temperature



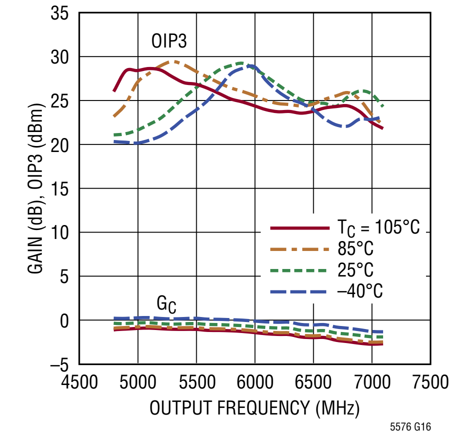
TYPICAL AC PERFORMANCE CHARACTERISTICS

5V, 5800MHz Output Frequency: T_C = 25°C. V_{CC} = 5V, EN = High, P_{IN} = –10dBm (–10dBm/Tone for 2-tone tests, Δf = 2MHz), P_{LO} = 0dBm, f_{IN} = 900MHz, f_{LO} = f_{OUT} – f_{IN}, unless otherwise noted. Test circuit shown in Figure 1.

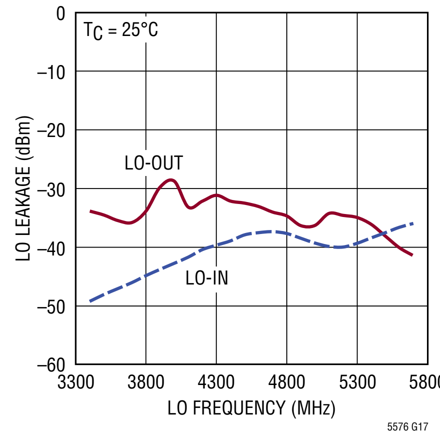
Conversion Gain, OIP3 and NF vs Input Frequency



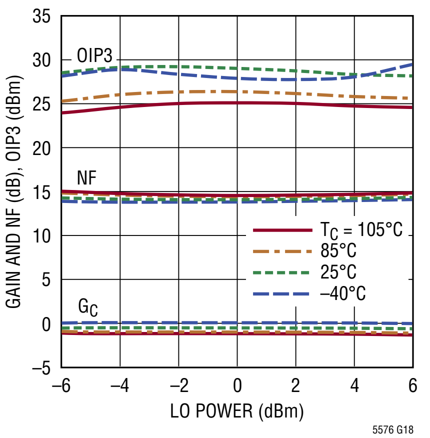
Conversion Gain and OIP3 vs Output Frequency



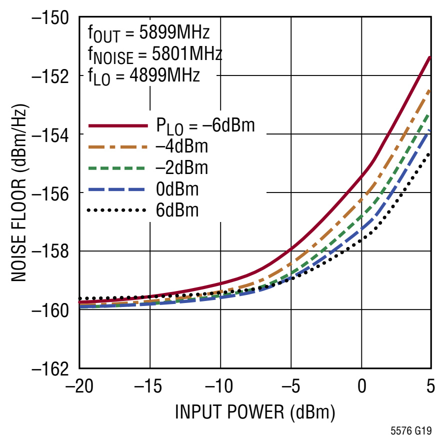
LO Leakage vs LO Frequency



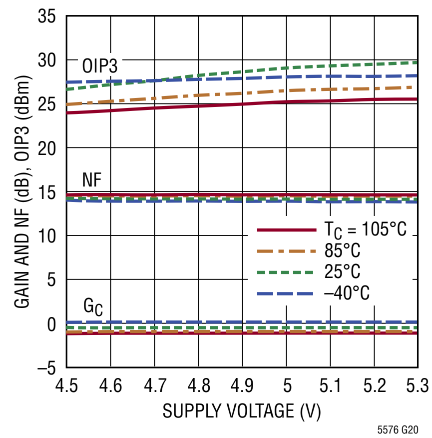
Conversion Gain, OIP3 and NF vs LO Input Power



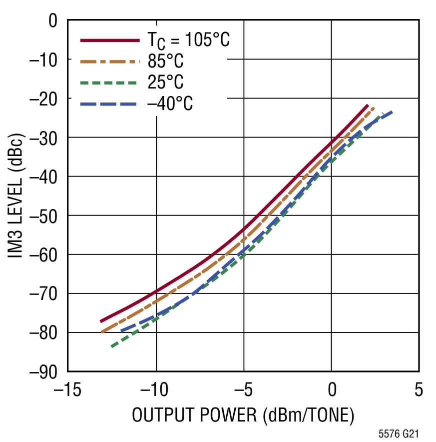
Output Noise Floor vs Input Power



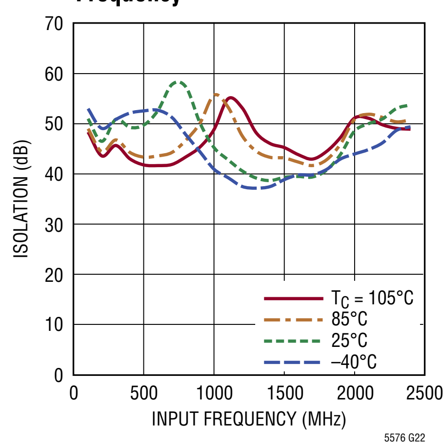
Conversion Gain, OIP3 and NF vs Supply Voltage



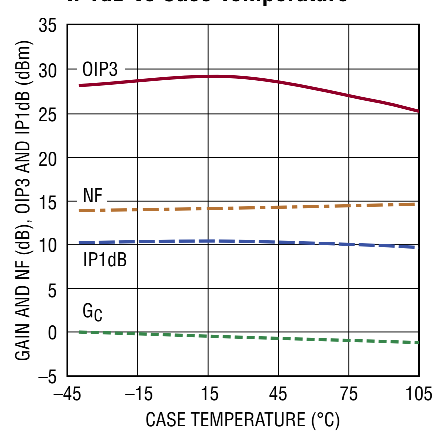
2-Tone IM3 Level vs Output Power Level



IN-OUT Isolation vs Input Frequency



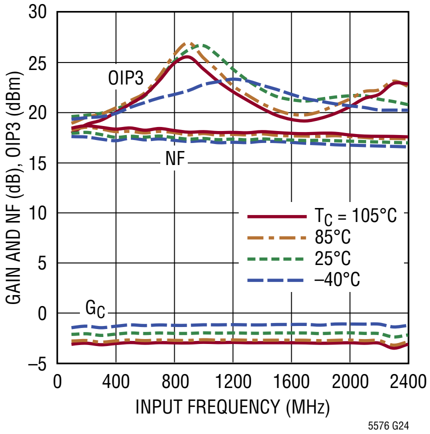
Conversion Gain, OIP3, NF and IP1dB vs Case Temperature



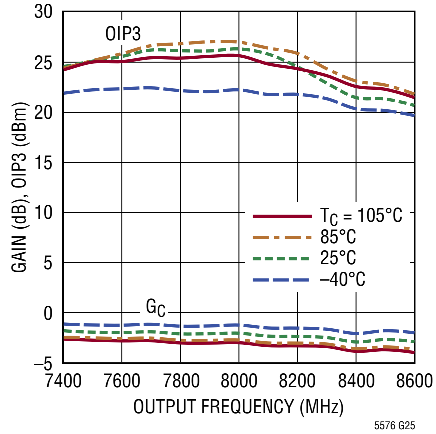
TYPICAL AC PERFORMANCE CHARACTERISTICS

5V, 8000MHz Output Frequency: T_C = 25°C. V_{CC} = 5V, EN = High, P_{IN} = –10dBm (–10dBm/Tone for 2-tone tests, Δf = 2MHz), P_{LO} = –4dBm, f_{IN} = 900MHz, f_{LO} = f_{OUT} – f_{IN}, unless otherwise noted. Test circuit shown in Figure 1.

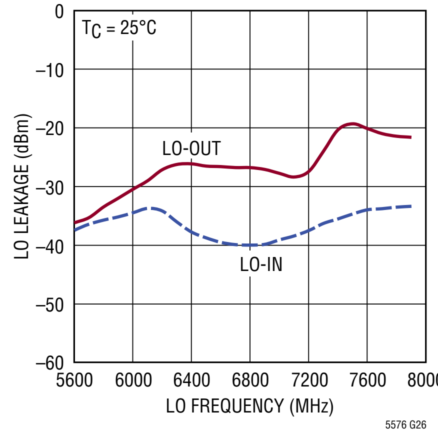
Conversion Gain, OIP3 and NF vs Input Frequency



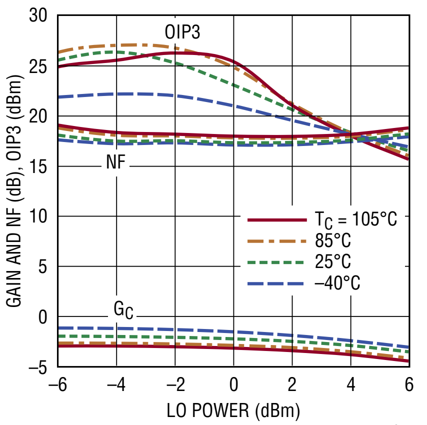
Conversion Gain and OIP3 vs Output Frequency



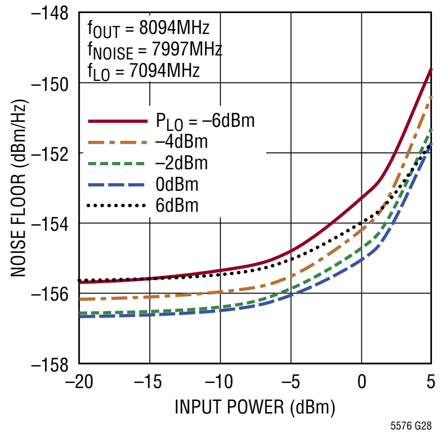
LO Leakage vs LO Frequency



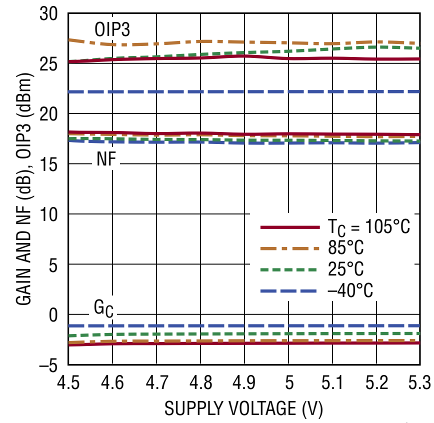
Conversion Gain, OIP3 and NF vs LO Input Power



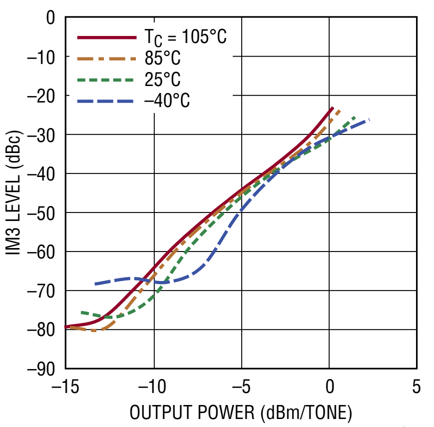
Output Noise Floor vs Input Power



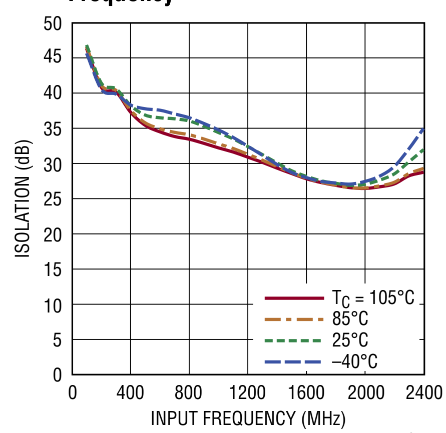
Conversion Gain, OIP3 and NF vs Supply Voltage



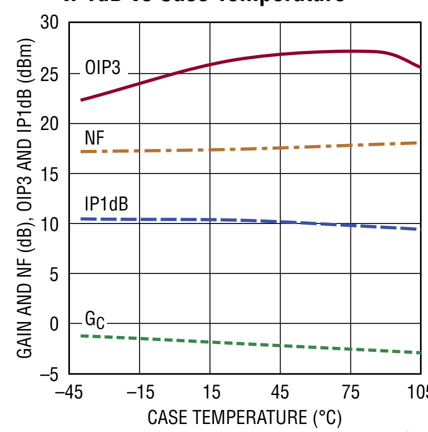
2-Tone IM3 Level vs Output Power Level



IN-OUT Isolation vs Input Frequency



Conversion Gain, OIP3, NF and IP1dB vs Case Temperature



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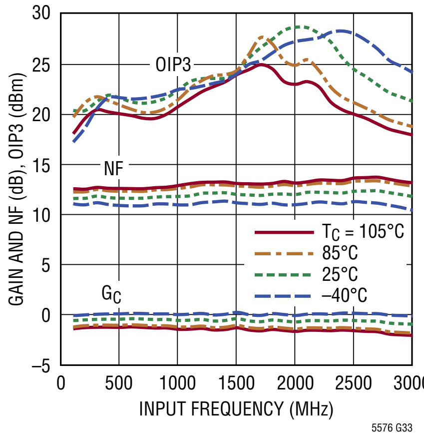
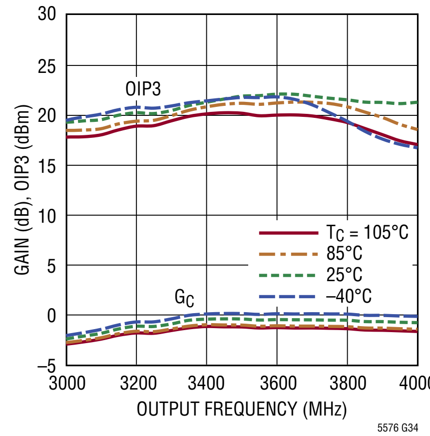
TYPICAL AC PERFORMANCE CHARACTERISTICS

3.3V, 3500MHz Output Frequency: T_C = 25°C. V_{CC} = 3.3V, EN = High, P_{IN} = –10dBm (–10dBm/Tone for 2-tone tests, Δf = 2MHz), P_{LO} = 0dBm, f_{IN} = 456MHz, f_{LO} = f_{OUT} – f_{IN}, unless otherwise noted. Test circuit shown in Figure 1.

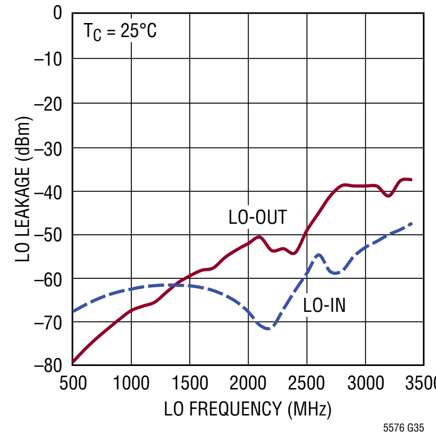
Conversion Gain, OIP3 and NF vs Input Frequency



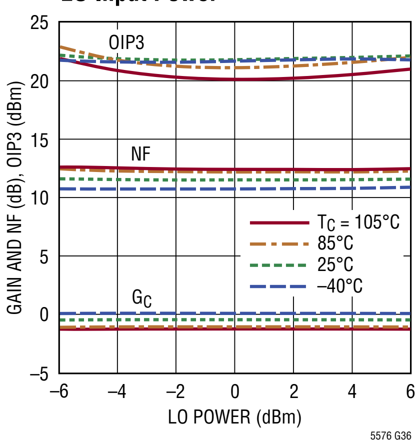
Conversion Gain and OIP3 vs Output Frequency



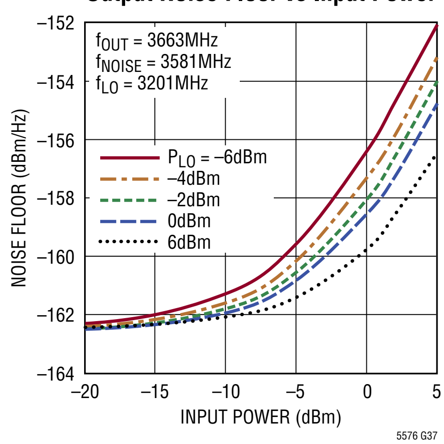
LO Leakage vs LO Frequency



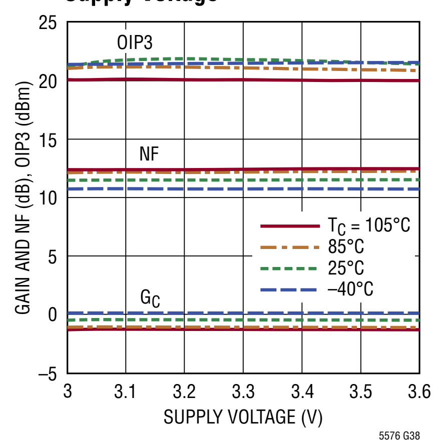
Conversion Gain, OIP3 and NF vs LO Input Power



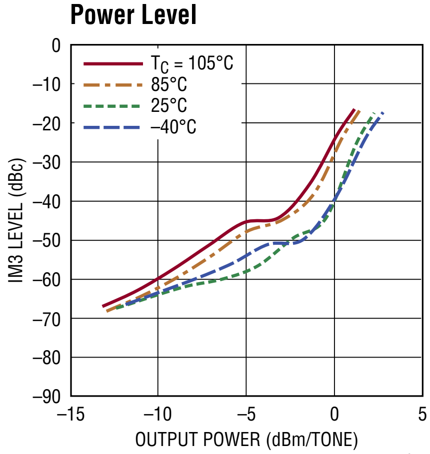
Output Noise Floor vs Input Power



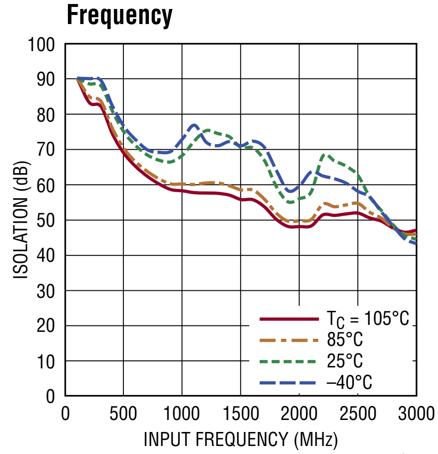
Conversion Gain, OIP3 and NF vs Supply Voltage



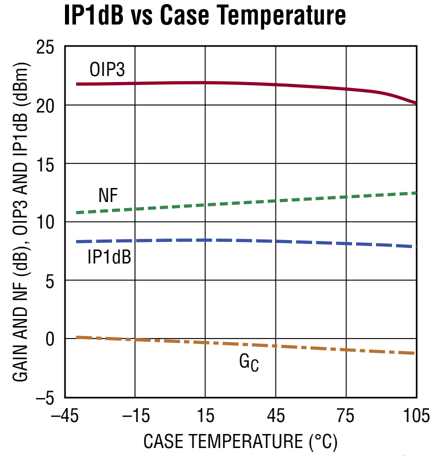
2-Tone IM3 Level vs Output Power Level



IN-OUT Isolation vs Input Frequency



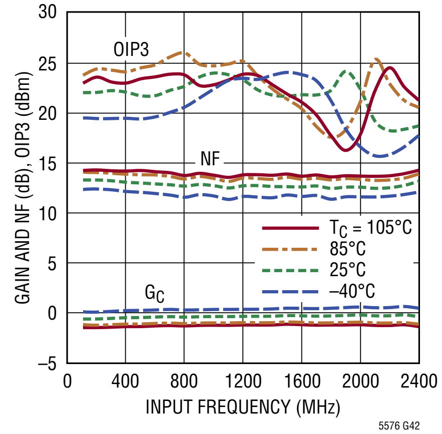
Conversion Gain, OIP3, NF and IP1dB vs Case Temperature



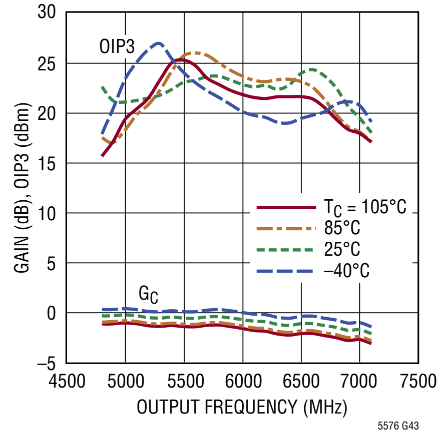
TYPICAL AC PERFORMANCE CHARACTERISTICS

3.3V, 5800MHz Output Frequency: T_C = 25°C. V_{CC} = 3.3V, EN = High, P_{IN} = –10dBm (–10dBm/Tone for 2-tone tests, Δf = 2MHz), P_{LO} = 0dBm, f_{IN} = 900MHz, f_{LO} = f_{OUT} – f_{IN}, unless otherwise noted. Test circuit shown in Figure 1.

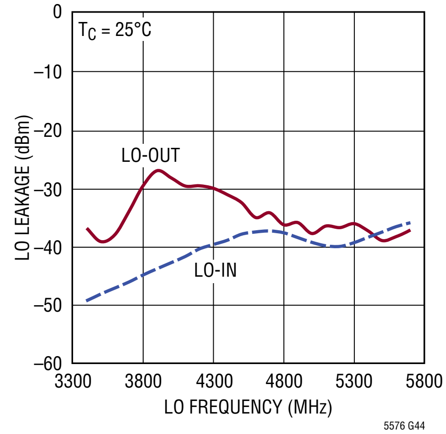
Conversion Gain, OIP3 and NF vs Input Frequency



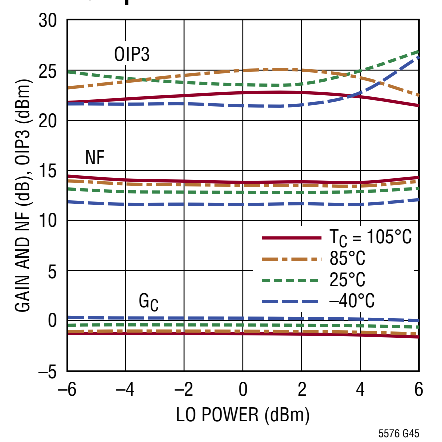
Conversion Gain and OIP3 vs Output Frequency



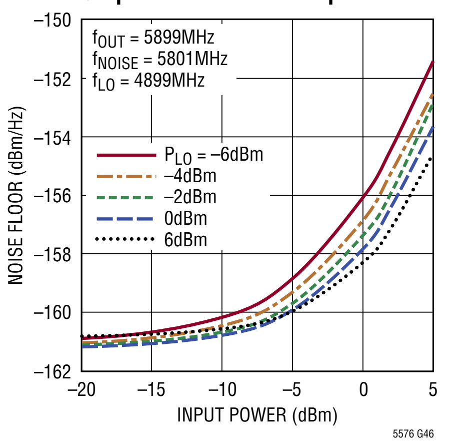
LO Leakage vs LO Frequency



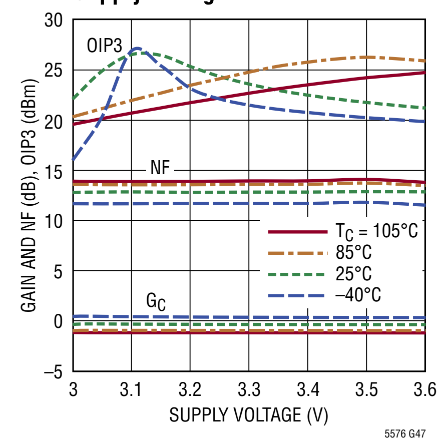
Conversion Gain, OIP3 and NF vs LO Input Power



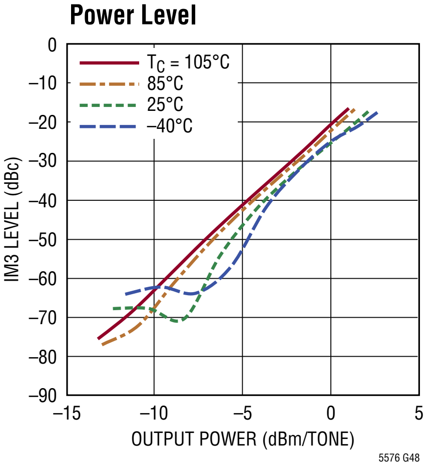
Output Noise Floor vs Input Power



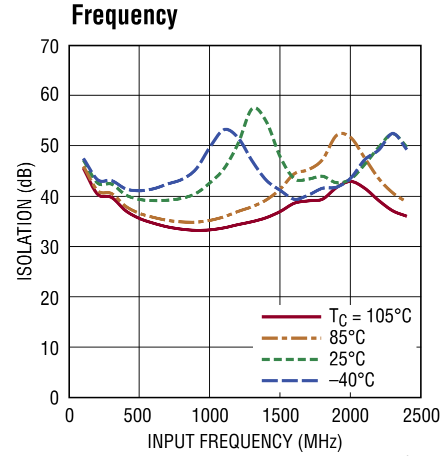
Conversion Gain, OIP3 and NF vs Supply Voltage



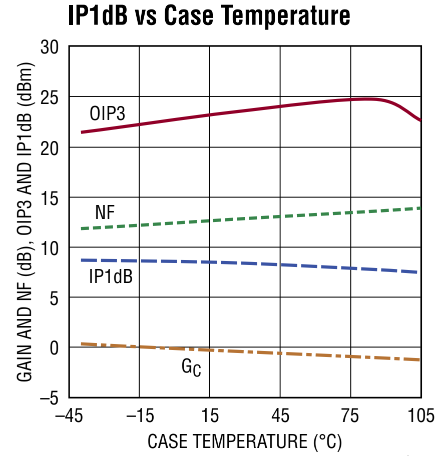
2-Tone IM3 Level vs Output Power Level



IN-OUT Isolation vs Input Frequency



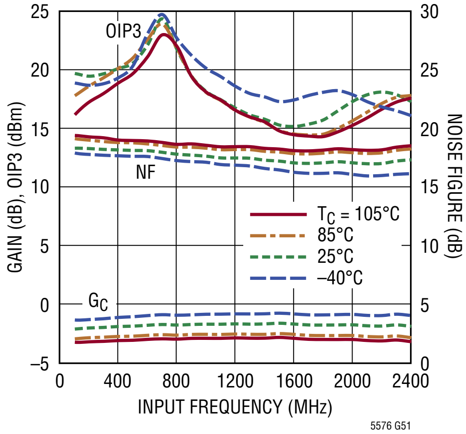
Conversion Gain, OIP3, NF and IP1dB vs Case Temperature



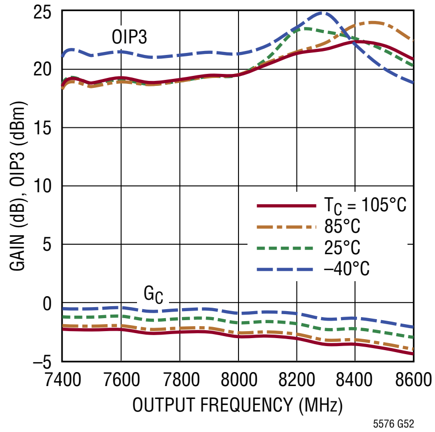
TYPICAL AC PERFORMANCE CHARACTERISTICS

3.3V, 8000MHz Output Frequency: T_C = 25°C. V_{CC} = 3.3V, EN = High, P_{IN} = –10dBm (–10dBm/Tone for 2-tone tests, Δf = 2MHz), P_{LO} = –4dBm, f_{IN} = 900MHz, f_{LO} = f_{OUT} – f_{IN}, unless otherwise noted. Test circuit shown in Figure 1.

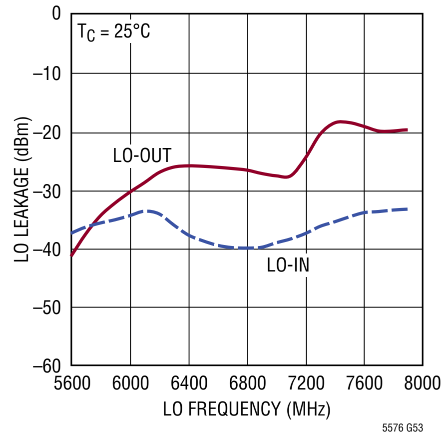
Conversion Gain, OIP3 and NF vs Input Frequency



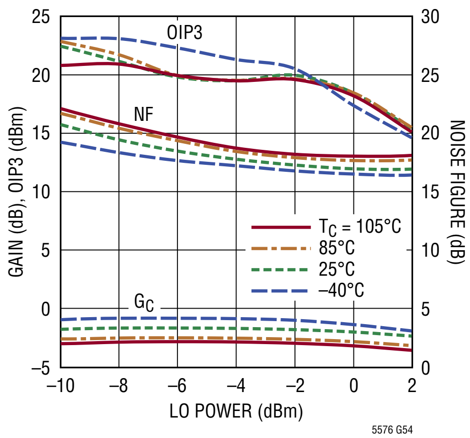
Conversion Gain and OIP3 vs Output Frequency



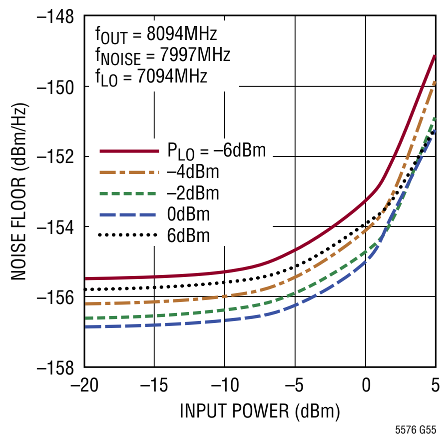
LO Leakage vs LO Frequency



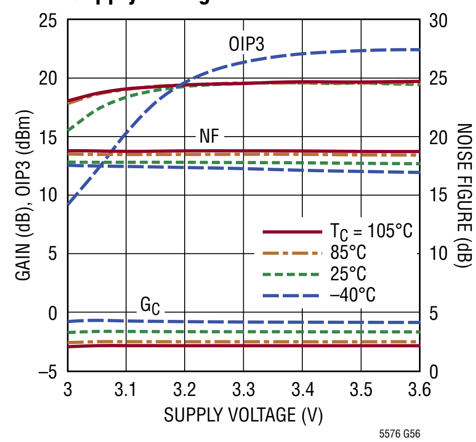
Conversion Gain, OIP3 and NF vs LO Input Power



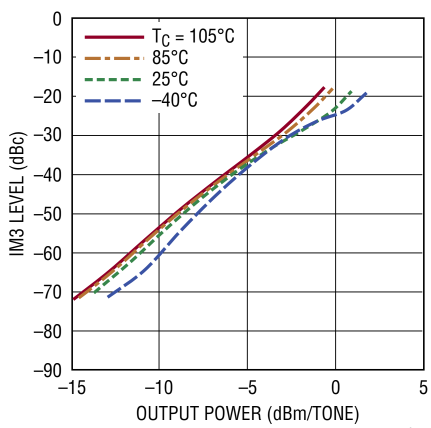
Output Noise Floor vs Input Power



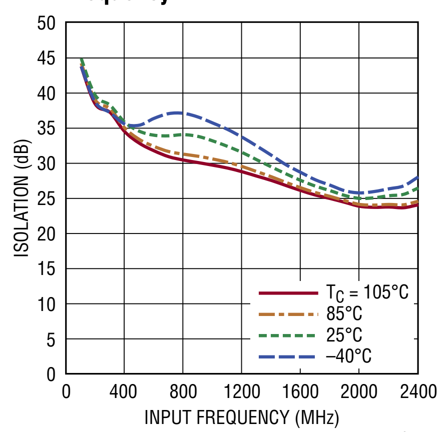
Conversion Gain, OIP3 and NF vs Supply Voltage



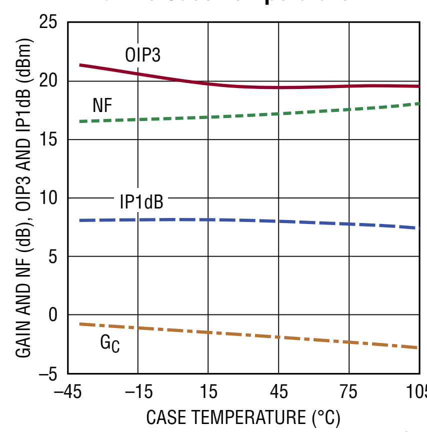
2-Tone IM3 Level vs Output Power Level



IN-OUT Isolation vs Input Frequency



Conversion Gain, OIP3, NF and IP1dB vs Case Temperature



5576f

PIN FUNCTIONS

TEMP (Pin 1): Temperature Monitor. This pin is connected to the anode of a diode through a 30Ω resistor. It may be used to measure the die temperature by forcing a current into the pin and measuring the resulting pin voltage.

IN+, IN– (Pins 2, 3): Differential Signal Input. For optimum performance these pins should be driven with a differential signal. The input can be driven single-ended with some performance degradation by connecting the unused pin to RF ground through a capacitor. An internally generated 1.6V DC bias voltage is present on these pins, thus DC blocking is required.

LGND (Pin 4): DC Ground Return for the Input Amplifier. This pin must be connected to a good DC and RF ground. The typical current from this pin is 64mA. In some applications, an external chip inductor may be used, though any DC resistance will reduce current in the mixer core, which could affect performance.

EN (Pin 5): Enable Pin. The IC is enabled when the applied voltage on this pin is greater than 1.8V. An applied voltage less than 0.5V will disable the IC. An internal 300k resistor pulls this pin low if it is left floating.

V_{CC} (Pins 6, 7): Power Supply Pin: These pins should be connected together on the circuit board and bypassed with a 10nF capacitor located close to the IC. (See the Auto Supply Voltage Detection and Supply Voltage Ramping sections for additional information).

IADJ (Pin 8): Bias Current Adjust Pin: This pin allows adjustment of the internal mixer current by adding an external pull-down resistor. The typical DC voltage on this pin is 1.8V. If not used, this pin must be left floating.

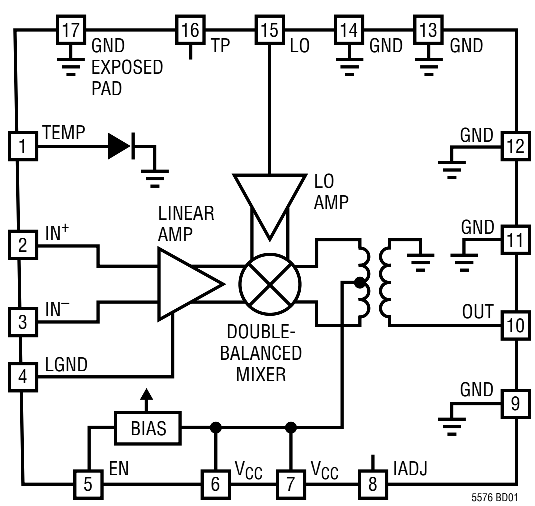
GND (Pins 9, 11, 12, 13, 14, 17 (Exposed Pad)): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad on the package provides both electrical contact to the ground and a good thermal contact to the printed circuit board.

OUT (Pin 10): Single-Ended Output Pin. This pin is connected internally to a single-ended transformer output. A DC voltage should not be applied to this pin. External components may be needed for impedance matching.

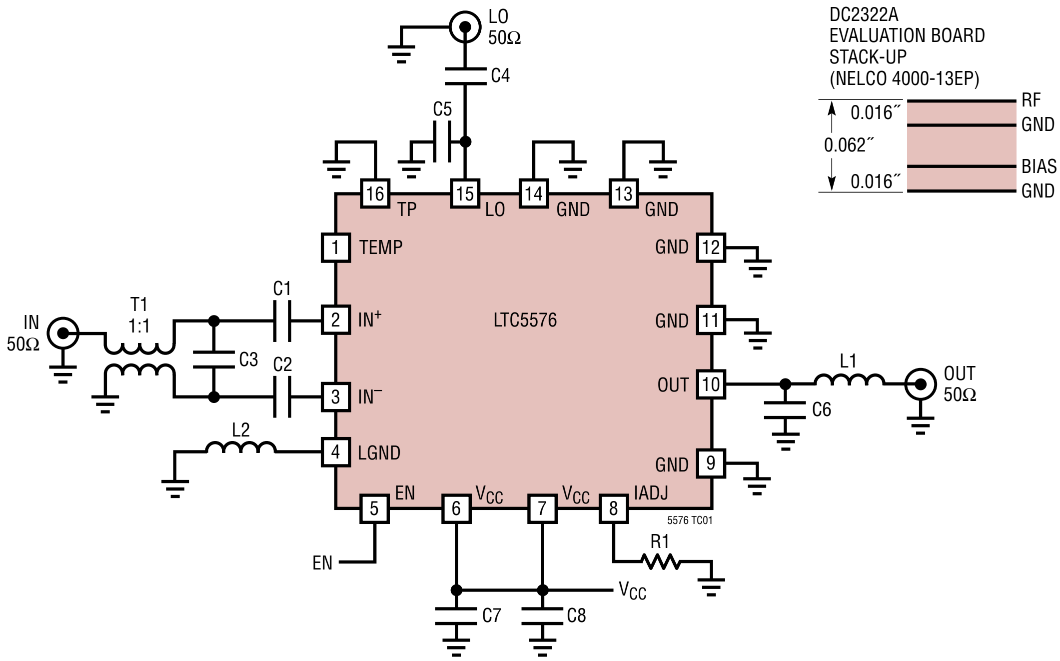
LO (Pin 15): Single-Ended LO Input. This pin is impedance matched over a broad frequency range. It is internally biased at 1.7V, thus a DC blocking capacitor is required.

TP (Pin 16): Test Pin: This pin is used for production test purposes only and must be connected to ground.

BLOCK DIAGRAM



TEST CIRCUIT



REF DES	VALUE	SIZE	VENDOR
C1, C2	1000pF	0402	Murata GRM
C3	See Table	0402	Murata GJM
C4	100pF	0402	Murata GRM
C5	0.3pF	0402	AVX Accu-P
C6	See Table	0402	AVX Accu-P
C7	10nF	0402	Murata GRM
C8	1µF	0603	Murata GRM
L1	See Table	0402	Coilcraft HP
L2	0Ω	0402	Vishay
R1	See Table	0402	Vishay
T1	1:1, 4.5MHz to 3000MHz	AT224-1	Mini-Circuits

OUTPUT FREQUENCY	C3	C6	L1	R1 (5V)	R1 (3.3V)
3500MHz	0.7pF	6.8nH (L)	0.5pF (C)	2.61kΩ, 1%	511Ω, 1%
5800MHz	-	0.2pF	0Ω	2.61kΩ, 1%	649Ω, 1%
8000MHz	-	0.2pF	1nH	2.61kΩ, 1%	649Ω, 1%

Figure 1. Test Circuit Schematic

APPLICATIONS INFORMATION

Introduction

The LTC5576 uses a high performance LO buffer amplifier driving a double-balanced mixer core to achieve frequency conversion with high linearity. A differential common-emitter stage at the mixer input allows very broad band matching of the input. The Block Diagram and Pin Functions sections provide additional details. The LTC5576 is primarily intended for upmixer applications, however, due to its broadband input capability, it could be used as a downmixer as well.

The test circuit schematic in Figure 1 shows the external component values used for the IC characterization. The evaluation board layout is shown in Figure 2. Additional components may be used to optimize performance for different applications.

The single-ended LO port is impedance matched over a very broad frequency range for ease of use. Low side or high side LO injection can be used, though the value of R1 may need to be adjusted accordingly for best performance. The IC includes an internal RF balun at the mixer output, thus the OUT port is single-ended. External components are required to optimize the impedance match for the desired frequency range.

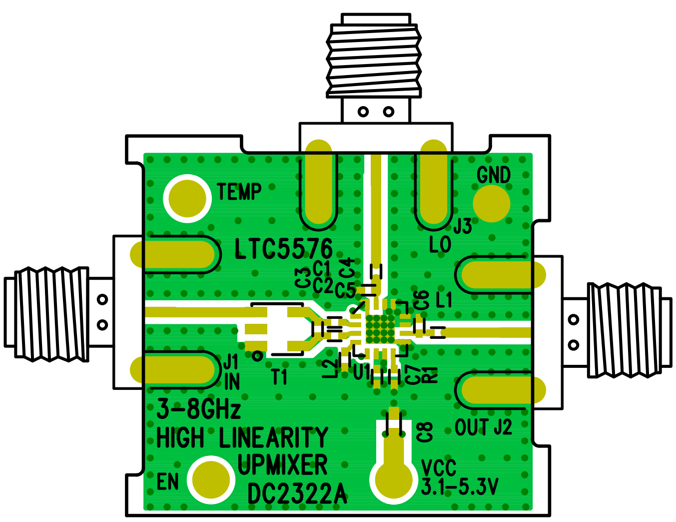


Figure 2. LTC5576 Evaluation Board Layout

IN Port

A simplified schematic of the mixer's input path is shown in Figure 3. The IN^+ and IN^- pins drive the bases of the input transistors while internal R-C networks are used for impedance matching. The input pins are internally biased to a common-mode voltage of 1.6V, thus external DC blocking capacitors, C1 and C2 are required. A small value of C3 can be used to extend the impedance match to higher frequencies. The 1:1 transformer provides single-ended to differential signal conversion for optimum performance.

Single-ended operation is possible by driving one input pin and connecting the unused input pin to RF ground through a capacitor. The performance will be degraded but may be acceptable at lower frequencies.

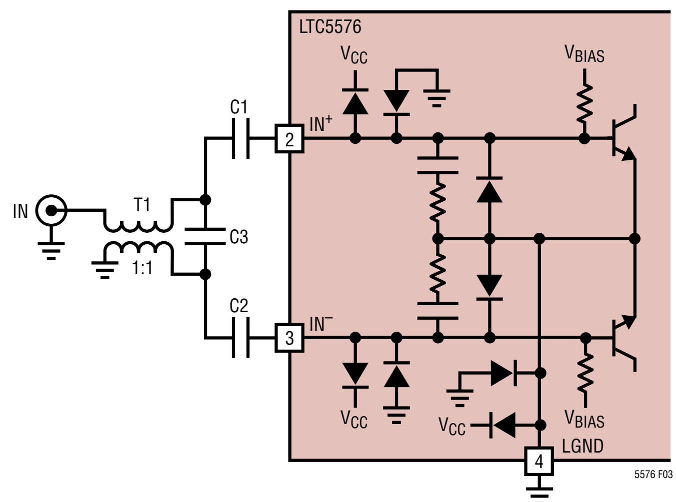


Figure 3. IN Port with External Matching

APPLICATIONS INFORMATION

Figure 4 shows the typical return loss at the IN port of the evaluation board with C1 and C2 values of 1000pF. The curves illustrate that adding a C3 value of 0.7pF improves the return loss at higher frequencies.

Differential reflection coefficients and impedances for the IN port are listed vs frequency in Table 1.

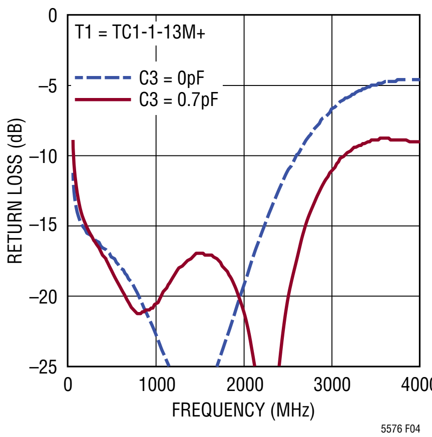


Figure 4. IN Port Return Loss

Table 1. IN Port Differential Impedance vs Frequency

FREQUENCY (MHz)	IMPEDANCE (Ω)		REFL. COEFF.	
	REAL*	IMAG*	MAG	ANG (°)
0.2	823	–j3971	0.89	–1.4
1	751	–j800	0.88	–7.2
10	133	–j154	0.50	–41
30	78.1	–j248	0.25	–36
50	73.3	–j378	0.20	–27
100	71.3	–j665	0.18	–17
200	70.7	–j961	0.17	–12
500	70.0	–j832	0.17	–14
1000	67.9	–j509	0.16	–24
1200	66.7	–j439	0.16	–28
1500	64.6	–j367	0.15	–35
2000	60.4	–j302	0.13	–49
2200	58.5	–j289	0.12	–55
2500	55.5	–j280	0.11	–66
3000	50.6	–j303	0.08	–91
4000	42.9	–j7460	0.08	–178
5000	42.7	j155	0.17	126
6000	55.9	j89	0.29	96

*Parallel Equivalent Impedance

The tail current of the input amplifier stage flows through pin 4 (LGND). Typically, this pin should be connected directly to a good RF ground; however, at lower input frequencies, it may be beneficial to insert an inductor to ground for improved IP2 performance. To minimize the inductors effect on DC current, the inductor should have low DC resistance. The expected current from this pin is approximately 64mA and any DC resistance on this pin will reduce the current in the mixer core which could adversely impact performance. The value of R1 can be adjusted to account for L1's DC resistance.

LO Port

The LTC5576 uses a single-ended LO signal to drive an input of a bipolar differential amplifier, as shown in Figure 5. The diff-pair provides single-ended to differential conversion to drive the mixer core. Internal resistors provide a broad band impedance match of 50Ω that is maintained when the part is disabled. The LO pin is biased internally to 1.7V, thus an external DC blocking capacitor (C4) is required. Optional capacitor, C5, can be used to improve the return loss at higher frequencies if needed.

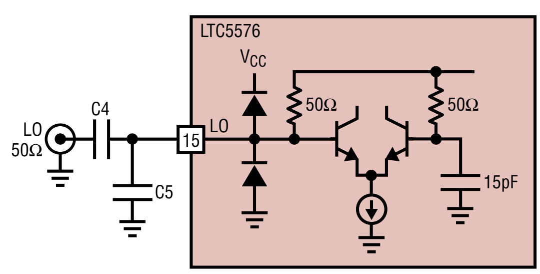


Figure 5. LO Port with External Matching

APPLICATIONS INFORMATION

Measured return loss of the LO port is shown in Figure 6 for a C4 value of 100pF. Without C5, the return loss is better than 10dB from 100MHz to beyond 4GHz. The addition of 0.3pF at C5 extends the 10dB match to beyond 8GHz.

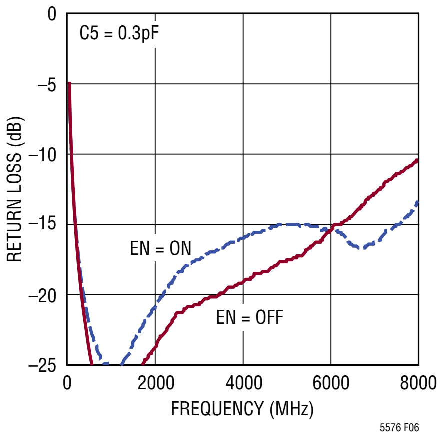


Figure 6. LO Port Return Loss

OUT Port

The LTC5576 uses an on-chip balun to provide a single-ended output, as shown in Figure 7. The output is optimized for 4GHz to 6GHz applications, but may be used for output frequencies as low as 3GHz, and as high as 8GHz.

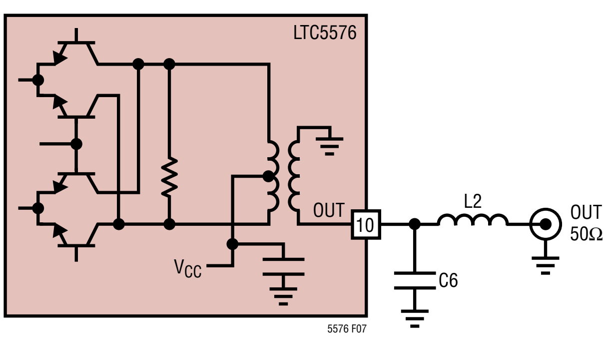


Figure 7. OUT Port with External Matching

External components C6 and L2 are used to optimize the impedance for the desired frequency range. High-Q components should be used here to minimize the impact on conversion gain. Table 2 lists the single-ended reflection coefficients and impedances of the OUT port and Table 3 lists component values for several application frequencies. In Figure 8, return loss is plotted for several of these values.

Table 2. OUT Port Impedance vs Frequency

FREQ (MHz)	IMPEDANCE (Ω)		REFL COEFF	
	REAL*	IMAG*	MAG	ANGLE
2500	12.8	51.8	0.78	86
3000	24.9	68.1	0.72	68
3500	50.7	80.7	0.63	51
4000	94.6	61.6	0.48	31
4500	89.5	4.7	0.29	5
5000	55.8	–8.0	0.09	–50
5500	38.7	–2.0	0.13	–169
6000	32.0	6.6	0.23	155
6500	30.6	16.5	0.31	128
7000	34.1	27.9	0.36	101
7500	41.2	39.4	0.41	79
8000	51.1	51.7	0.46	62
8500	62.5	57.7	0.47	51

*Series Impedance: Z = REAL + jIMAG

Table 3. Output Component Values

FREQ (MHz)	12dB RL BAND (MHz)	VALUES	
		C6	L2
3000	2800 to 3200	Open	0.5pF (C)
3500	3360 to 3830	6.8nH (L)	0.5pF (C)
5000	4000 to 6700	3.3nH (L)	0.6pF (C)
5200	4700 to 5800	Open	0Ω
5800	4870 to 7040	0.2pF	0Ω
8000	7500 to 8700	0.2pF	1nH

APPLICATIONS INFORMATION

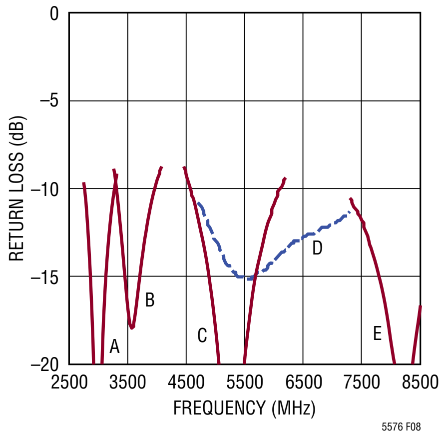


Figure 8. OUT Port Return Loss Tuned for (A) 3000MHz, (B) 3500MHz, (C) 5200MHz, (D) 5800MHz, (E) 8000MHz

DC and RF Grounding

The LTC5576 relies on the backside ground of the package for both RF and thermal performance. The exposed pad must be soldered to the low impedance topside ground plane of the board. The topside ground should also be connected to other ground layers to aid in thermal dissipation and ensure a low inductance RF ground. The LTC5576 evaluation board (Figure 2) utilizes a four by four array of vias under the exposed pad for this purpose.

Enable Interface

Figure 9 shows a simplified schematic of the EN interface. To enable the part, the applied EN voltage must be greater than 1.8V. Setting the voltage to below 0.5V will disable the IC. If the enable function is not required, the enable pin can be connected directly to V_{CC}. If the enable pin is left floating, an internal 300k pull-down resistor will disable the IC.

The voltage at the enable pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V, otherwise supply current may be sourced through the upper ESD diode. Under no circumstances should voltage be applied to the enable pin before the supply voltage is applied to the V_{CC} pin. If this occurs, damage to the IC may result.

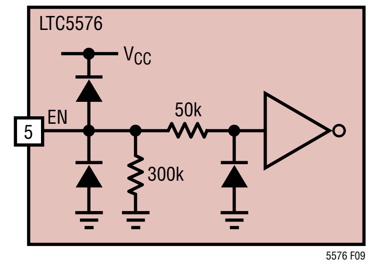


Figure 9. EN Pin Interface

Current Adjust Pin (IADJ)

The IADJ pin (Pin 8) can be used to optimize the performance of the mixer. The nominal open-circuit DC voltage on this pin is 1.8V and the typical short-circuit current is 1.9mA. As shown in Figure 10, an internal 4mA reference sets the current in the mixer core. Connecting R1 to the IADJ pin shunts some of this current to ground, thus reducing the mixer core current. The optimum value of R1 depends on the supply voltage and LO injection (low side or high side). Some recommended values are shown in Table 4 but the values can be optimized as required for individual applications.

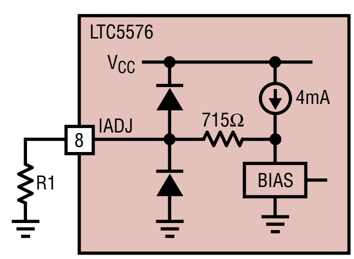


Figure 10. Current Adjust Pin Interface

APPLICATIONS INFORMATION

Table 4. Recommended R1 Values

V_{CC} (V)	f_{IN} (MHz)	f_{OUT} (MHz)	f_{LO} (MHz)	R1 (Ω)
3.3	456	3500	3044	511
3.3	900	5800	4900	649
3.3	900	8000	7100	649
5.0	456	3500	3044	2.61k
5.0	900	5800	4900	2.61k
5.0	1300	5000	6300	2.61K

Temperature Monitor Pin (TEMP)

The TEMP pin (pin 1) is connected to an on-chip diode that can be used as a coarse temperature monitor by forcing current into it and measuring the resulting voltage. The temperature diode is protected by a series 30Ω resistor and additional ESD diodes to ground. The TEMP pin voltage is shown as a function of junction temperature in Figure 11.

Given the voltage at the pin, V_{TEMP}, (in mV) the junction temperature in °C can be estimated for forced input currents of 10μA and 80μA using the following equations:

$$T_J(10\mu A) = (742.4 - V_{TEMP})/1.796$$

$$T_J(80\mu A) = (795.6 - V_{TEMP})/1.609$$

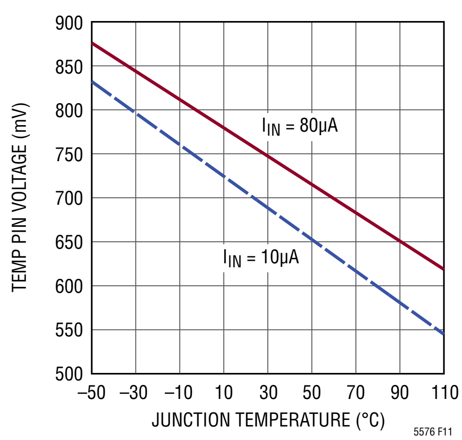


Figure 11. TEMP Pin Voltage vs Junction Temperature

Auto Supply Voltage Detection

An internal circuit automatically detects the supply voltage and configures internal components for 3.3V or 5V operation. The DC current is affected when the auto-detect circuit switches at approximately 4.1V. **To avoid undesired operation, the mixer should only be operated in the 3.1V to 3.6V or 4.5V to 5.3V supply ranges.**

Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

It is recommended that the EN pin be used to enable or disable the LTC5576 with V_{CC} held constant. However, if the EN pin and V_{CC} are switched simultaneously, then the configuration shown in Figure 12 is recommended. A maximum V_{CC} ramp rate at pins 6 and 7 of 20V/ms is recommended.

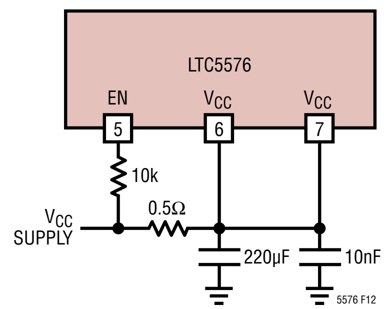


Figure 12. Suggested Configuration for Simultaneous V_{CC} and EN Switching

Spurious Output Levels

Mixer spurious output levels vs harmonics of the IN and LO frequencies are tabulated in Tables 5 and 6 for the 5V, 5800MHz application. Results are shown for spur frequencies up to 18GHz. The spur frequencies can be calculated using the following equation:

$$f_{SPUR} = |M \cdot f_{IN} \pm N \cdot f_{LO}|$$

Table 5 lists the *difference* spurs ($f_{SPUR} = |M \cdot f_{IN} - N \cdot f_{LO}|$) and Table 6 lists the *sum* spurs ($f_{SPUR} = |M \cdot f_{IN} + N \cdot f_{LO}|$). The spur levels were measured on a standard evaluation board at room temperature using the test circuit of Figure 1.

The spurious output levels for any application will be dependent on the external matching circuits and the particular application frequencies.

APPLICATIONS INFORMATION

Table 5. Output Spur Levels (dBc), $f_{SPUR} = |M \cdot f_{IN} - N \cdot f_{LO}|$ (f_{IN} = 900MHz, f_{OUT} = 5.8GHz, Low Side LO at 0dBm)

		N					
		0	**1**	**2**	**3**	**4**	**5**
M	**0**	–	–22.4	2.3	–24.6		
	1	–56.3	–0.8	–38.5	–34.6		
	2	–72.3	–51.9	–49.7	–68.6	–81.1	
	3	–81.9	–75.7	–76.7	–69.7	*	
	4	*	*	*	*	*	
	5	*	*	*	*	*	
	6	*	*	*	*	*	
	7	*	*	*	*	*	
	8	*	*	*	*	*	*
	9	*	*	*	*	*	*
	10	*	*	*	*	*	*

*Less Than –90dBc

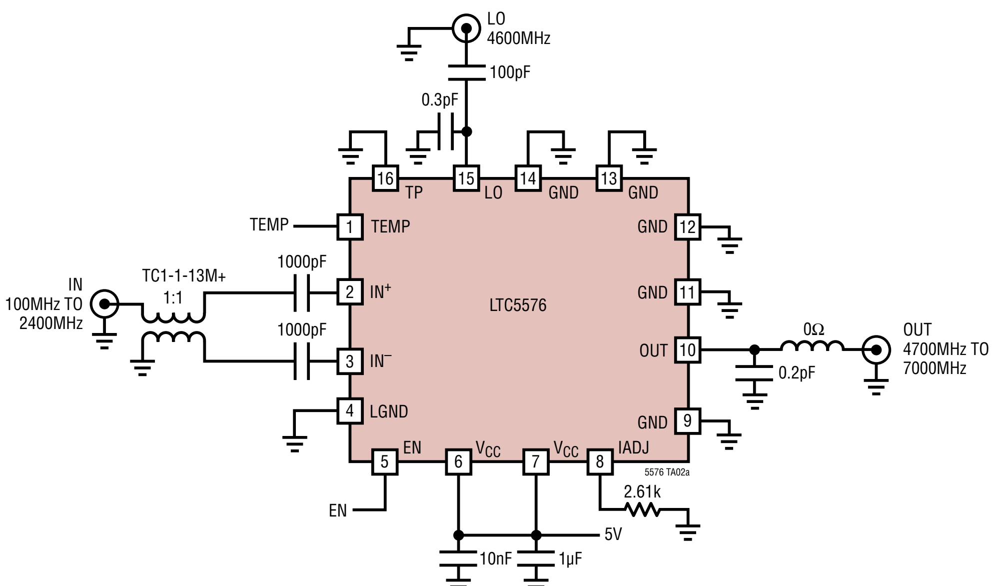
Table 6. Output Spur Levels (dBc), $f_{SPUR} = |M \cdot f_{IN} + N \cdot f_{LO}|$ (f_{IN} = 900MHz, f_{OUT} = 5.8GHz, Low Side LO at 0dBm)

		N					
		0	**1**	**2**	**3**	**4**	**5**
M	**0**	–	–22.4	2.3	–24.7		
	1	–56.3	0.0	–39.3	–39.5		
	2	–72.2	–49.2	–45.6	–73.4		
	3	-81.9	–71.7	–82.6	*		
	4	*	*	–87.0			
	5	*	*	*			
	6	*	*	*			
	7	*	*	*			
	8	*	*	*			
	9	*	*	*			
	10	*	*				

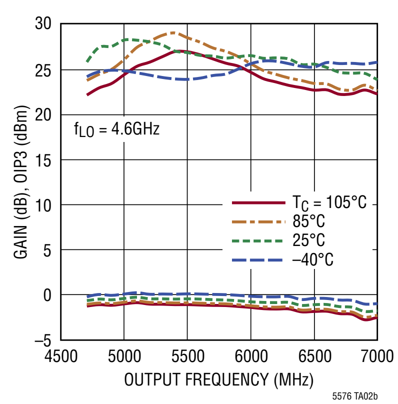
*Less Than –90dBc

TYPICAL APPLICATIONS

1.2GHz to 5.8GHz Upmixer with 2.3GHz Bandwidth

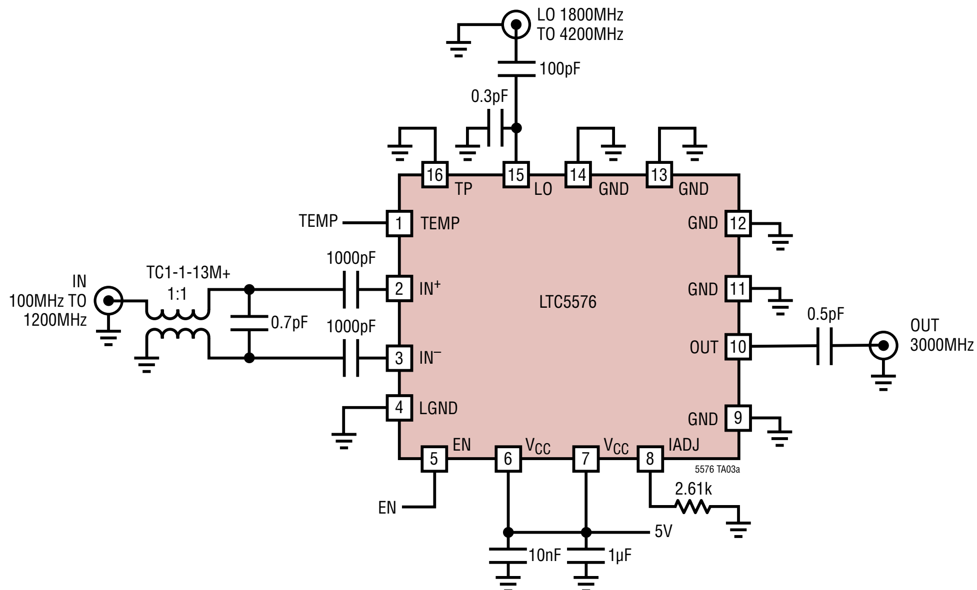


Conversion Gain and OIP3 vs Output Frequency

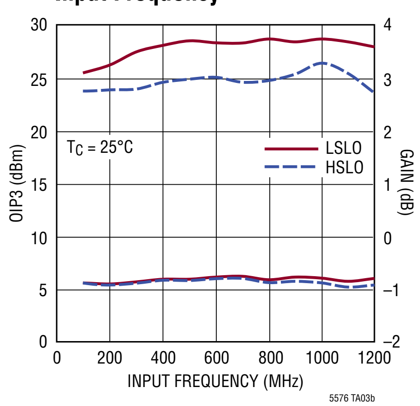


TYPICAL APPLICATIONS

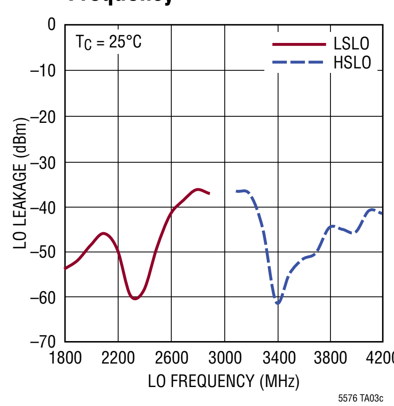
Upmixer with Broadband Input and 3GHz Output



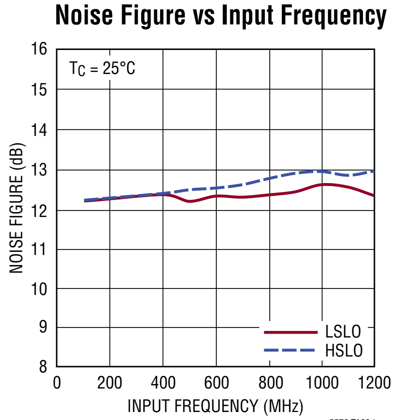
Conversion Gain and OIP3 vs Input Frequency



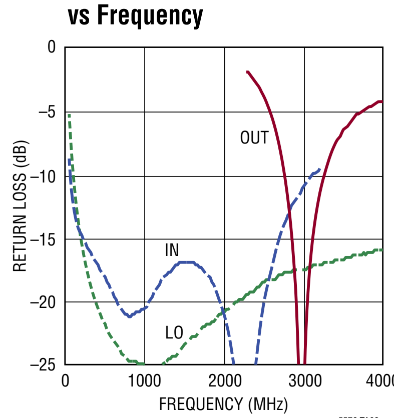
LO-OUT Leakage vs LO Frequency



Noise Figure vs Input Frequency

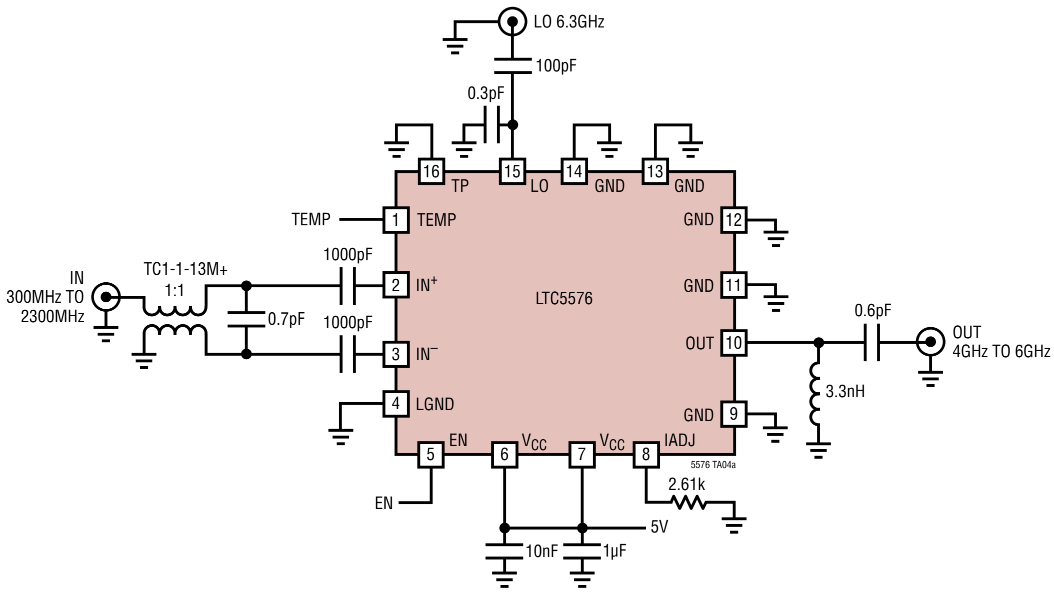


IN, OUT and LO Port Return Loss vs Frequency

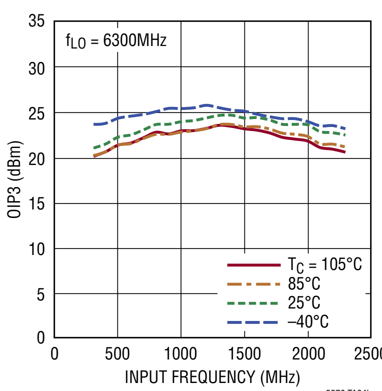


TYPICAL APPLICATIONS

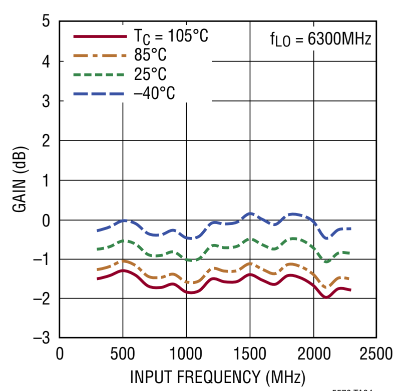
Broadband 4GHz to 6GHz Output Matching with Fixed LO Frequency (High Side LO)



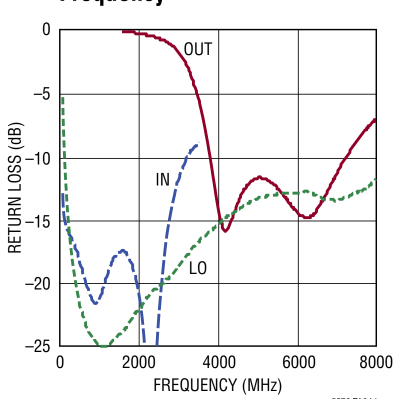
OIP3 vs Input Frequency



Conversion Gain vs Input Frequency

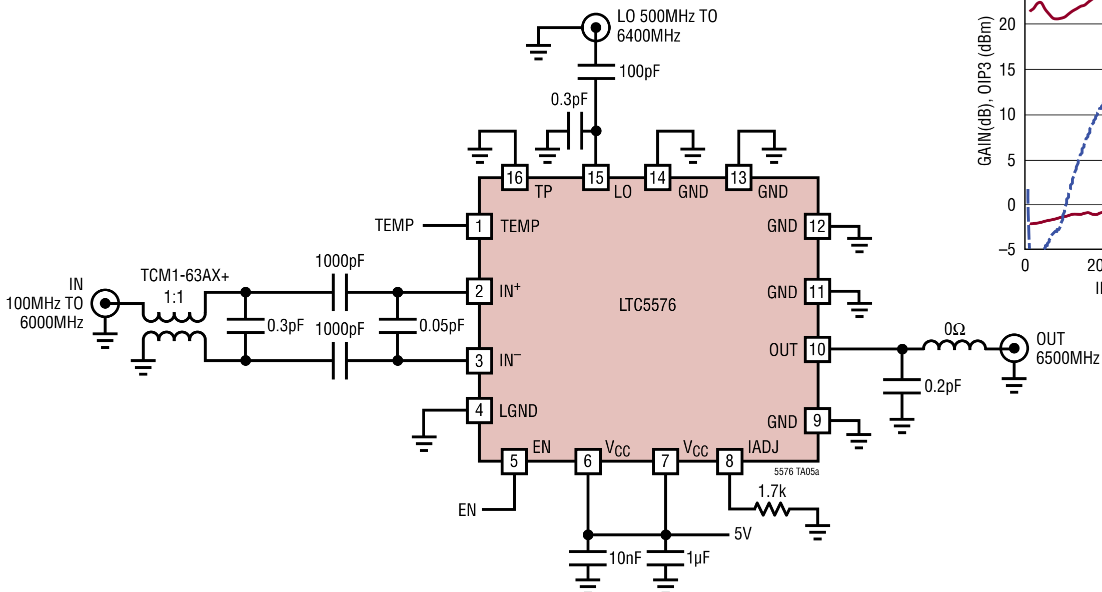


IN, OUT and LO Return Loss vs Frequency

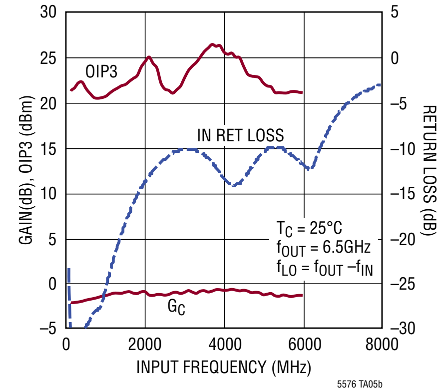


TYPICAL APPLICATIONS

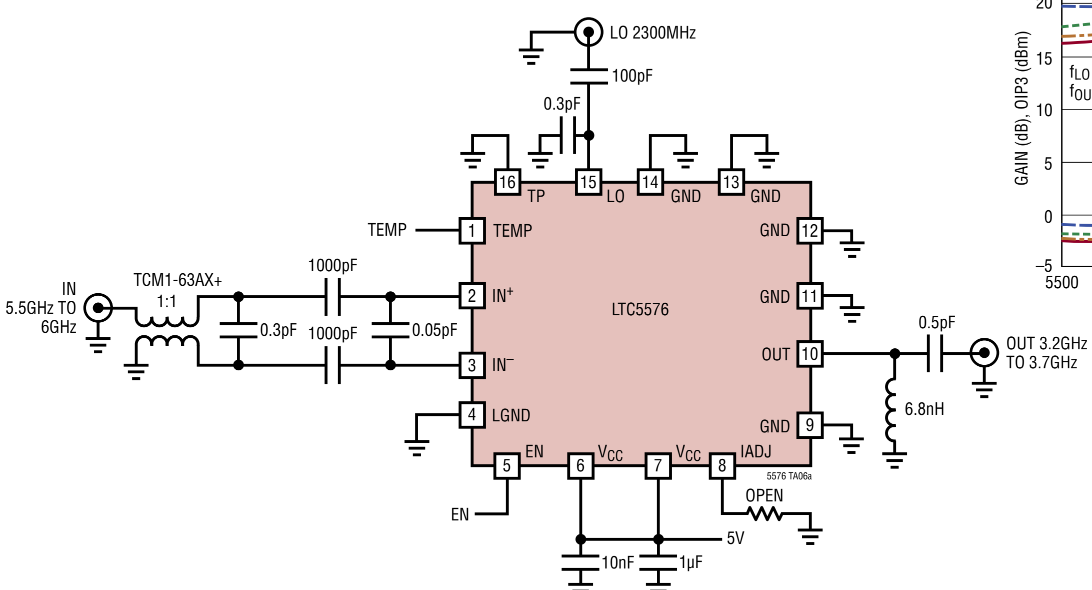
Very Broadband 100MHz to 6GHz Input Matching with 6.5GHz Output and Low Side LO



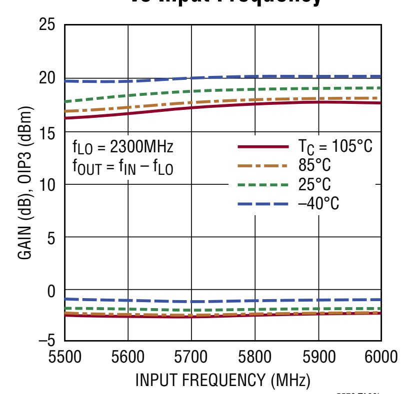
Conversion Gain, OIP3 and IN Return Loss vs Input Frequency



Downmixer Applications, 5.8GHz to 3.5GHz with Low Side LO



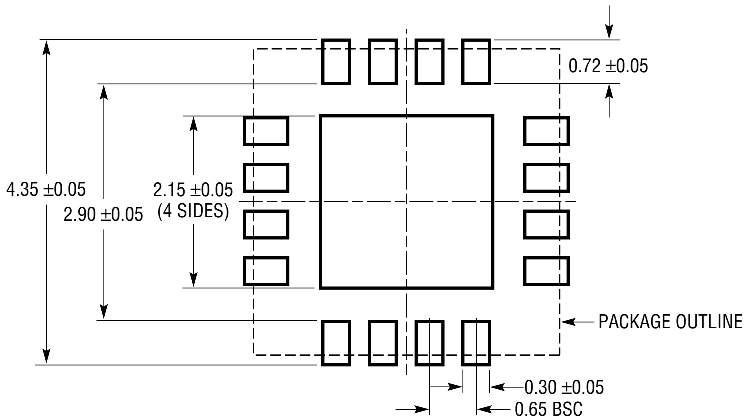
Conversion Gain and OIP3 vs Input Frequency



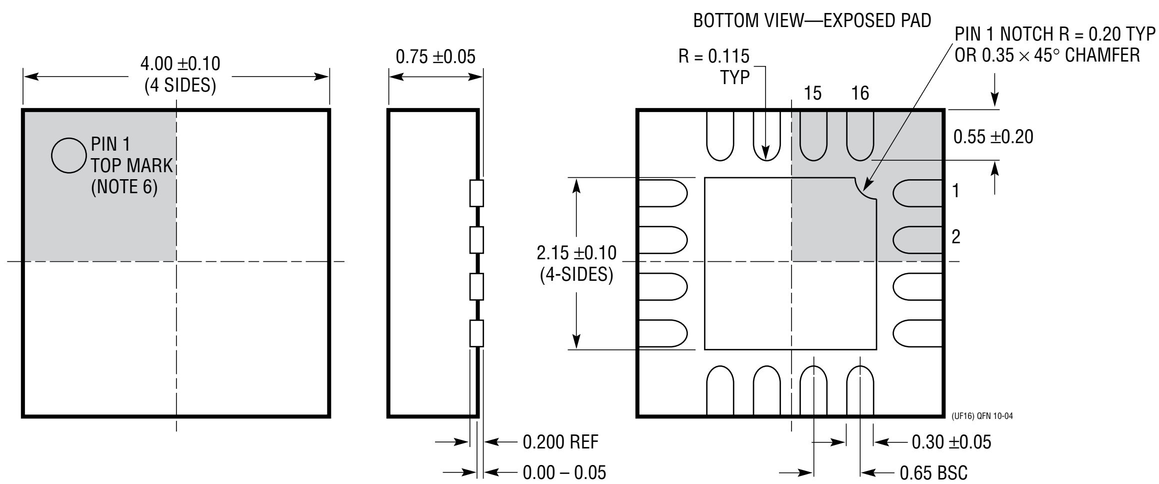
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692 Rev Ø)



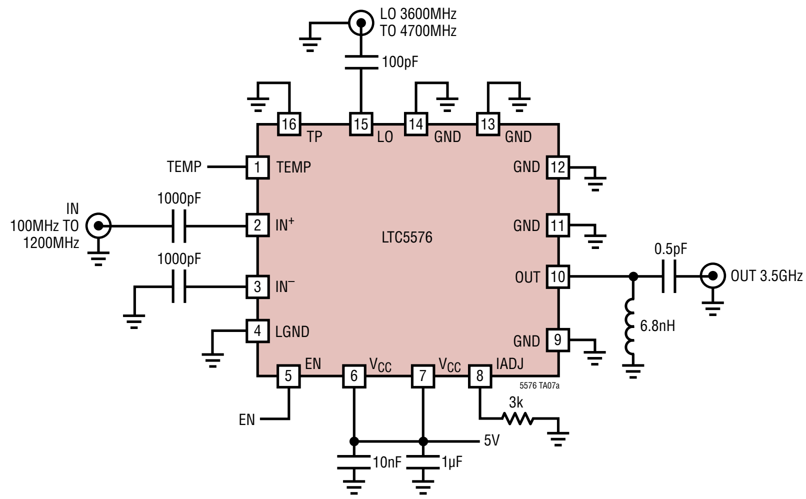
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



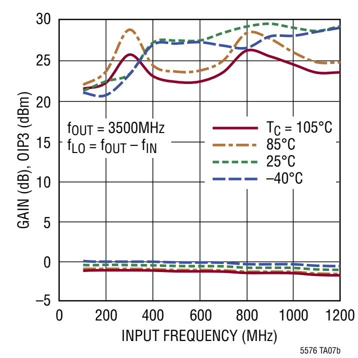
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Single-Ended Input with 3.5GHz Output



Gain and OIP3 vs Input Frequency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Mixers and Modulators		
LTC5510	1MHz to 6MHz, Wideband High Linearity Active Mixer	1.5dB Gain, Up and Downconversion, 3.3V or 5V Supply
LT®5578	400MHz to 2.7GHz Upconverting Mixer	27dBm OIP3 at 900MHz, 24.2dBm at 1.95GHz, Integrated RF Output Transformer
LT5579	1.5GHz to 3.8GHz Upconverting Mixer	27.3dBm OIP3 at 2.14GHz, NF = 9.9dB, 3.3V Supply, Single-Ended LO and RF Ports
LTC5577	300MHz to 6GHz High Signal Level Active Downconverting Mixer	0dB Gain, 30dBm IIP3 and 15dBm Input P1dB, 3.3V/180mA Supply
LTC5551	300MHz to 3.5GHz Ultra High Dynamic Range Downconverting Mixer	36dBm IIP3, 2.4dB Gain, 9.7dB NF, 0dBm LO Drive, 18dBm P1dB
LTC5544	4GHz to 6GHz, 3.3V High Gain Downconverting Mixer	24dB Gain, 25.9dBm IIP3 and 11.3dB NF at 5.25GHz, 3.3V/194mA Supply
LTC5588-1	200MHz to 6GHz I/Q Modulator	31dBm OIP3 at 2.14GHz, –160.6dBm/Hz Noise Floor
LTC5585	700MHz to 3GHz Wideband I/Q Demodulator	>530MHz Demodulation Bandwidth, IIP2 Tunable to >80dBm, DC Offset Nulling
Amplifiers		
LTC6430-15	High Linearity Differential IF Amp	20MHz to 2GHz Bandwidth, 15.2dB Gain, 50dBm OIP3, 3dB NF at 240MHz
LTC6431-15	High Linearity Single-Ended IF Amp	20MHz to 1.7GHz Bandwidth, 15.5dB Gain, 47dBm OIP3, 3.3dB NF at 240MHz
LTC6412	31dB Linear Analog VGA	35dBm OIP3 at 240MHz, Continuous Gain Range –14dB to 17dB
LT5554	Ultralow Distortion IF Digital VGA	48dBm OIP3 at 200MHz, 2dB to 18dB Gain Range, 0.125dB Gain Steps
RF Power Detectors		
LT5538	40MHz to 3.8GHz Log Detector	±0.8dB Accuracy Over Temperature, –72dBm Sensitivity, 75dB Dynamic Range
LT5581	6GHz Low Power RMS Detector	40dB Dynamic Range, ±1dB Accuracy Over Temperature, 1.5mA Supply Current
LTC5582	40MHz to 10GHz RMS Detector	±0.5dB Accuracy Over Temperature, ±0.2dB Linearity Error, 57dB Dynamic Range
LTC5583	Dual 6GHz RMS Power Detector	Up to 60dB Dynamic Range, ±0.5dB Accuracy Over Temperature, >50dB Isolation
ADCs		
LTC2208	16-Bit, 130Msps ADC	78dBFS Noise Floor, >83dB SFDR at 250MHz
LTC2153-14	14-Bit, 310Msps Low Power ADC	68.8dBFS SNR, 88dB SFDR, 401mW Power Consumption
RF PLL/Synthesizer with VCO		
LTC6948	Low Noise, Low Spurious Fractional-N PLL with Integrated VCO	373MHz to 6.39GHz, –157dBc/Hz WB Phase Noise Floor, –108dBc/Hz Closed-Loop Phase Noise

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